REMARKS

In the Office Action, the Examiner rejected claims 1-6, 8-11, 13, 16-18, 20-27, 29, and 32-46. Claims 1-6, 8-11, 13, 16-18, 20-27, 29, and 32-46 remain pending in the present application and are believed to be in condition for allowance. By the present Response, Applicants amend claims 9, 32 and 36 to further clarify the claimed subject matter and added new claims 47 and 48. Upon entry of the amendments, claims 1-6, 8, 11, 13, 16-18, 20-27, 29 and 32-48 are pending in the present patent application. Applicants respectfully request reconsideration of the above-referenced application in view of the foregoing amendments and the following remarks.

Rejections under Section 103

The Examiner rejected claims 1-23 and 25-29 under 35 U.S.C. 103(a) as being unpatentable over Leung et al (U.S. Patent No. 6,272,577, hereafter referred to as "the Leung reference") in view of Guttag (U.S. Patent No. 5,761,726, hereafter referred to as "the Guttag reference"). Claims 33-38 were also rejected under 35 U.S.C. 103(a) as being unpatenable over Leung in view of Guttag and further in view of Gupta (U.S. Patent No. 6,405,286, hereafter referred to as "the Gupta refernce"). Additionally, claim 32 was rejected under 35 U.S.C. 103(a) as being unpatentable over the Gupta reference in view of Blaner (U.S.Patent No. 5,737, 575, hereafter "the Blaner reference").

The rationale for the rejection of claim 1 was incorporated by the Examiner into the rejection of each rejection of independent claims 9, 16, 25, 33 and 36. In rejecting claim 1, the Examiner stated, in pertinent part:

> Leung does not specifically teach associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices as recited in the claim.
>
> Guttag discloses associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices [col. 172, lines 48-55] to generate addresses for read/write access to data stored within a plurality of memories (col. 5, ll. 40-45).

Office Action, pg. 8. Applicants respectfully traverse the rejection.

Legal Precedent

First, the burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). In addressing obviousness determinations under 35 U.S.C. § 103, the Supreme Court in *KSR International Co. v. Teleflex Inc.*, No. 04-1350 (April 30, 2007), reaffirmed many of its precedents relating to obviousness including its holding in *Graham v. John Deere Co.*, 383 U.S. 1 (1966). In *KSR*, the Court also reaffirmed that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *Id.* at 14. In this regard, the *KSR* court stated that "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does ... because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *Id.* at 14-15. In *KSR*, the court noted that the demonstration of a teaching, suggestion, or motivation to combine provides a "helpful insight" in determining whether claimed subject matter is obvious. *KSR, slip op.* at 14.

Moreover, the *KSR* court did not diminish the requirement for objective evidence of obviousness. *Id.* at 14 ("To facilitate review, this analysis should be made explict. *See In re Kahn,* 441 F.3d 977, 988 (CA Fed. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness"). As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ."); *see also, In re Lee,* 61 U.S.P.Q.2d 1430, 1436 (Fed. Cir. 2002) (holding that the factual inquiry whether to combine references must be thorough and searching, and that it must be based on *objective evidence of record*).

Additionally, the pending claims must be given an interpretation that is reasonable and consistent with the *specification*. *See In re Prater*, 162 U.S.P.Q. 541, 550-51 (C.C.P.A. 1969) (emphasis added); *see also In re Morris,* 44 U.S.P.Q.2d 1023, 1027-28 (Fed. Cir. 1997); *see also* M.P.E.P. §§ 608.01(o) and 2111. Indeed, the specification is "the primary basis for construing the claims." *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). As such, one should rely *heavily* on the written description for guidance as to the meaning of the claims. *See id.*

Furthermore, interpretation of the claims must also be consistent with the interpretation that *one of ordinary skill in the art* would reach. *See In re Cortright*, 49 U.S.P.Q.2d 1464, 1468 (Fed. Cir. 1999); M.P.E.P. § 2111. "The inquiry into how a person of ordinary skill in the art understands a claim term provides an objective baseline from

which to begin claim interpretation."[2] *See Collegenet, Inc. v. ApplyYourself, Inc.*, 75 U.S.P.Q.2d 1733, 1738 (Fed. Cir. 2005) (quoting *Phillips v. AWH Corp.*, 75 U.S.P.Q.2d 1321, 1326). The Federal Circuit has made clear that derivation of a claim term must be based on "usage in the ordinary and accustomed meaning of the words amongst artisans of ordinary skill in the relevant art." *See id.*

Independent Claims 1, 9, 16 and 25

Independent claim 1 recites, *inter alia,* "associating each of the plurality of target devices with *a single base address*, wherein *the same single base address is associated with each of the plurality of target devices*; sending a multicast transaction from the initiator device to the plurality of target devices, wherein sending the multicast transaction comprises sending a multicast transaction to *the single base address* associated with each of the plurality of target devices." (Emphasis added). Independent claim 9 recites, *inter alia*, "accessing a first portion of memory by a first target device in response to the multicast transaction request; and accessing a second portion of memory by a second target device concurrently with the access to the first portion of memory in response to the multicast transaction request, wherein the first and second portions of memory are accessed with *a single base address associated with both the first target device and the second target device, wherein the first target device and the second target device are associated with the same single base address.*" (Emphasis added). Independent claim 16 recites, *inter alia*, "a plurality of target devices coupled to the bus wherein each of the plurality of target devices concurrently executes a portion of the transaction request, wherein the initiator device is configured to multicast the transaction request to the plurality of target devices using *a single base address associated with the plurality of*

target devices, wherein the same single base address is associated with each of the plurality of target devices." (Emphasis added). Independent claim 25 recites, *inter alia,* "a plurality of target devices coupled to the bus, the plurality of target devices configured to execute the multicast transaction with concurrent data responses from a plurality of interleaved memory regions, wherein the initiator device is configured to multicast the transaction request to the plurality of target devices using *a single base address associated with the plurality of target devices, wherein the same single base address is associated with each of the plurality of target devices.*"

Applicants agree with the Examiner that the Leung reference fails to disclose the feature of the plurality of target devices having a single base address, wherein the *same single base address is associated with each of the plurality of target devices.* However, contrary to the Examiner's assertion, the Guttag reference does not overcome this admitted deficiency of the Leung reference. In particular, Guttag does not disclose a plurality of target devices with *a single base address*, wherein *the same single base address is associated with each of the plurality of target devices,* as set forth in claims 1, 9, 16 and 25.

The Guttag reference is directed to a multi-processing system that includes a plurality of memories and a plurality of processors. *See* Guttag, col. 5, lines 35-36. As stated in the Guttag reference:

> Each of the memories has a unique addressable memory portion of a single memory space. Each processor has a predetermined plurality of corresponding memories. These corresponding memories have a corresponding base address within said single memory address space.

Guttag, at col. 5, lines 36-41. In rejecting claim 1, the Examiner referred to col. 172, lines 48-55 (claim 1) from the Guttag reference as disclosing the above-recited claim features. In its entirety, the cited portion states:

> a plurality of n processors, where n is less than m and each of said n processors has a predetermined *plurality of corresponding memories*, said predetermined plurality of memories corresponding to *each processor having a corresponding fixed base address* within said single memory address space, each of said processors capable of generating any address within said single memory address space for read/write access to data stored within said plurality of m memories.

Guttag, col. 172, lines 48-55 (emphasis added). As the above-quoted sections clearly illustrate, the Guttag reference discloses each of a *plurality* of processors that each have *their own* (*i.e., corresponding*) base address within *their own individual section* of the memory address space. *See also*, Guttag, col. 172, lines 43-47 (disclosing a plurality of m memories within the address space, each memory having a "*unique* addressable memory portion"). Consequently, the claim feature "wherein *the same single base address* is associated with each of the plurality of target devices" is not taught by Guttag. Indeed, the Guttag reference teaches the antithesis of this feature in that each memory has its own, unique base address.

In light of the clear factual deficiencies of the Examiner's evidence, Applicants respectfully assert that the Examiner has not established a *prima facie* case of obviousness with regard to claims 1, 9, 16 or 25. Specifically, the Leung reference and the Guttag reference, taken alone or in hypothetical combination, do not disclose the features of independent claims 1, 9, 16 and 25. Accordingly, Applicants respectfully request

withdrawal of the pending Section 103 rejection and allowance of independent claims 1, 9, 16, and 25 and the claims that depend therefrom.

Independent Claims 33 and 36

As stated above, in rejecting independent claims 33 and 36 as being unpatentable over the Leung reference in view of the Guttag reference and further in view of the Gupta reference, the Examiner incorporated the rationale of claim 1. Applicants respectfully traverse the rejection.

Claim 33 recites, *inter alia*, "associating the plurality of target devices with *a single base memory address*, wherein *the same single base memory address is associated with each of the plurality of target devices*." (Emphasis added). Amended claim 36 recites, *inter alia*, "code to configure the plurality of devices to *associate a single base address with the plurality of devices*, wherein *the same single base address is associated with each of the plurality of devices*." (Emphasis added).

The Examiner admitted in the rejection of claim 1 that the Leung reference fails to disclose a single base memory address being associated with each of the plurality of target devices. As set forth above, the Guttag reference clearly does not to overcome the deficiencies of the Leung reference in this regard. Specifically, the Guttag reference discloses a system wherein processors have unique base addresses within memory space. *See* Guttag, col . 172, lines 43-55. This is the antithesis of the claimed feature having the same single base address being associated with each of the plurality of devices. As such,

the Leung and Guttag references, alone or in combination, do not disclose all the features of the independent claims 33 and 36.

Applicants respectfully assert that the Gupta reference does not overcome this deficiency of the Leung and Guttag references. The Gupta reference discloses an interleaved memory coupled with a plurality of memory buses over which *independent memory transactions* may simultaneously be performed, but where only a single memory transaction can be active on a memory bus at any given time. *See* Gupta, abstract; col. 6, lines 19-29; col. 16, lines 17-23. However, the Gupta reference does not disclose that the same single base memory address is associated with each of a plurality of target devices, as set forth in claims 33 and 36. Accordingly, the Leung, Guttag and Gupta references, taken alone or in hypothetical combination, do not disclose all the features of independent claims 33 and 36.

As such, Applicants respectfully assert that a *prima facie* case of obviousness under Section 103 has not been established with regard to independent claims 33 and 36. Therefore, Applicants respectfully request withdrawal of the rejection under Section 103 and allowance of claims 33 and 36, as well as all claims depending therefrom.

Independent Claim 32

As mentioned above, claim 32 was rejected under Section 103 as being unpatentable over the Gupta reference in view of the Blaner reference. In the rejection, the Examiner stated:

> As per claim 32, Gupta discloses a computer comprising a memory [col. 1, lines 24-25]; a controller configured to logically divide the memory into a plurality of interleaved memory regions [Fig. 2]; and a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices simultaneously accesses its associated interleaved memory regions in response to a single transaction request [col. 6, lines 21-28; col. 16, ll 12-24].
>
> Gupta further discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request [two or more memory busses can each perform memory transactions simultaneously, with each memory bus coupled to one or more memory bus segments, wherein a single memory transaction can be active on a single memory bus segment at any given time, and each memory bus segment is coupled to one or more interleaved memory banks; col. 16, ll 15-23]
>
> Blaner incontestably discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests [interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access; col. 8, ll 22-26] to allow simultaneous access to multiple pages of memory and reduce latency (col. 2, ll 65-67).

Office Action pgs. 17-18. Applicants respectfully traverse the rejection.

Amended claim 32 recites, *inter alia*, "a plurality of devices having a *common base address*, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices *simultaneously accesses* its associated interleaved memory region *in response to a single transaction request directed to the common base address.*" (Emphasis added).

Applicants respectfully assert that the Gupta reference fails to disclose all the elements of claim 32 and, further, that the Blaner reference fails to obviate the deficiencies

of the Gupta reference. First, with regard to the Gupta reference, contrary to the Examiner's assertions, does not disclose a plurality of devices simultaneously accessing associated interleaved memory regions in *response to a single transaction*. As discussed above, the Gupta reference is directed to a system wherein the memory is accessed simultaneously in response to *multiple transactions*. Indeed, the portions of the Gupta reference relied on by the Examiner only disclose multiple simultaneous transactions resulting in simultaneous memory access with only a single transaction per bus at any one time. *See* Gupta, col. 6, lines 21-28; col. 16, lines 12-24. However, the Applicants are unaware of anything in the Gupta reference that can even remotely be considered as disclosing, teaching or suggesting a plurality of devices simultaneously accessing interleaved memory in response to *a single transaction*.

Additionally, there is nothing in Gupta with respect to the plurality of devices having a *common base address* and simultaneous access of the plurality of devices to associated interleaved memory region in response to *a single transaction request directed to the common base address*. The Blaner reference does not overcome the deficiencies of the Gupta reference in this respect.

The Blaner reference is directed to the processing of storage keys in a computer that employs key-controlled storage protection. *See* Balaner, col. 1, lines 32-35. The two main features of the system in Blaner are 1) interleaved memory and 2) an associateive multi-page key cache. *See id.* at col. 4, lines 60-64. The interleaved memory physically stores the keys in separate RAMs so that address A addresses the key for page p and the address A+1 addresses the key for page p+n. *See id.* at col. 4, line 64 through col. 5, line

1. According to Blaner, this organization allows for n keys of a plurality of pages to be fetched in one access. *See id.* at col. 5, lines 1-2. However, there is no mention in the Blaner reference of a plurality of devices having a common base address wherein where *each simultaneously accesses its associated interleaved memory region in response to a single transaction request directed to the common base address*, as set forth in claim 32. As such, the Gupta reference and the Blaner reference, taken alone or in combination, fail to disclose all the features of claim 32.

Accordingly, Applicants respectfully request withdrawal of the Section 103 rejection and allowance of claim 32. Accordingly, Applicants respectfully request that the Examiner withdraw the Section 103 rejection based on the Gupta reference and the Blaner reference and allow independent claim 32.

Claims 24 and 39-46

Applicants respectfully assert that the Examiner has not established a *prima facie* case of obviousness with regard to dependent claims 24 and 39-46. The Examiner rejected claim 24 as obvious over the Leung reference in view of the Guttag reference and the Carmichael reference and rejected claims 39-46 as obvious over the Leung reference in view of the Guttag reference and the Olarig reference. However, as described above, the Leung and Guttag references clearly do not disclose those claim features attributed by the Examiner in the rejection of the independent claims 1, 16, 25, and 32, upon which claims 24 and 39-44 depend, respectively. Additionally, the Gupta and Blaner references clearly do not disclose those claim features attributed by the Examiner in rejecting claim32, upon which claims 45 and 46 depend. In view of the deficiencies of the Leung, Guttag, Gupta

and Blaner references with respect to the independent claims, the Examiner's Section 103 rejections of claims 24 and 39-46, which are based upon the Examiner's mistaken interpretation of these references, cannot establish a *prima facie* case of obviousness. As such, Applicants respectfully request withdrawal of the Section 103 rejections of claims 24 and 39-46.

Conclusion

Applicants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner wishes to resolve any other issues by way of a telephone conference, the Examiner is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: October 25, 2007

Michael G. Fletcher
Registration No. 32,777
(281) 970-4545

Correspondence Address:
IP Administration
Legal Department, M/S 35
HEWLETT-PACKARD COMPANY
P.O. Box 272400
Fort Collins, CO 80527-2400